First Named Inventor	Frankie F. Roohparvar
Serial No.	09/608,580
Filing Date	June 30, 2000
Group Art Unit	2818
Examiner Name	Trong Q. Phan
Confirmation No.	9345
Attorney Docket No.	400.006US01

EXAMINER INTERVIEW SUMMARY

#15 3/31/03

Title: ZERO LATENCY-ZERO BUS TURNAROUND SYNCHRONOUS FLASH MEMORY

Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

In a telephonic conversation with the Examiner on March 19, 2003, with the below-signed attorney, Andrew C. Walseth, no agreement was reached regarding the pending claims. The Examiner maintained that a system having a Flash memory coupled with a synchronous serial I/O or processor having a clock inherently implied that the Flash memory was also synchronous and thus anticipated the claims. The Examiner also stated that further search would be required if the claims were amended to include the limitation of a Flash memory with a SDRAM or other specific synchronous interface.

The Examiner is invited to contact Applicant's Representatives at direct dial (612) 312-2207 if there are any changes or questions regarding this Examiner Interview Summary or if prosecution of this application may be assisted thereby.

Respectfully submitted,

Date: 3/24/03

Andrew C. Walseth
Reg. No. 43,234

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